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| 09/836,834 | 04/17/2001 | Donald M. Gray III | 14531.101 | 9966 |

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|---|
| MEW, KEVIN D |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2664 | |

DATE MAILED: 03/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| | Application No. | Applicant(s) |
| :-- | :-- | :-- |
| **Office Action Summary** | 09/836,834 | GRAY ET AL. |
| | Examiner | Art Unit |
| | Kevin Mew | 2664 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1)☒ Responsive to communication(s) filed on *17 April 2001*.

2a)☐ This action is **FINAL**.    2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

## Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date *1*.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

## *Detailed Action*

## *Specification*

1.      The disclosure is objected to because of the following informalities:

Label 702, which is designated for the variable delay interface, is mislabeled as 703 on

line 6 of paragraph 0068, page 22 of the specification.

Label 913, which is designated for the time base, is mislabeled as 613 on the last line of

paragraph 0076, page 25 of the specification.

Appropriate correction is required.

## *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2.      Claims 1-4, 6-8, 10-12, 14-15, 17-18 are rejected under 35 U.S.C. 102(e) as being

anticipated by Ishibashi (USP 6,778,537).

Regarding claim 1, Ishibashi discloses in a network system that includes a multimedia

source (a plurality of program data multiplexed onto a single transport stream, see col. 6, lines

47-54) and a multimedia sink (DTV, see col. 6, lines 18-28, 40-46 and Fig. 1), the multimedia

source transmitting a stream of multimedia packets (a single transport stream of program data,

see col. 6, lines 47-54) to the multimedia sink (DTV, see col. 6, lines 18-28, 40-46 and Fig. 1)

over a plurality of heterogeneous networks (a system that comprises a plurality of nodes, see col.

6, lines 28-37), the heterogeneous networks including a plurality of variable delay networks(a

system that comprises a plurality of nodes, see col. 6, lines 28-37), a method of performing

constant delay communication of the stream of multimedia packets from the multimedia source

over the heterogeneous networks to the multimedia sink even though one or more of the

variable delay networks (all other nodes other than the node that comprises PC 1, see col. 6, lines

28-37) do not themselves provide for a common reckoning of time in the variable delay network

(these nodes do not provide common time reckoning and rely on the root node to provide

reference clock synchronization, see col. 6, lines 18-37 and Figs. 1 and 9), the method

comprising the following:

establishing a common time reckoning (reference clock) in all of the variable delay

networks (external nodes) that do not themselves provide for a common time reckoning (the

1394 interface section 13 of PC 1 has a timer function of clocking the same time as that of the

external node by making periodic adjustments to the external node on the basis of a reference

clock, see col. 6, lines 18-37 and Fig. 1; note that external nodes do not provide a common time

reckoning);

emulating the plurality of variable delay networks as one or more constant delay

networks (emulating a timing adjusting circuit (pacer) for the 1394 link of PC 1 in software, see

col. 2, lines 3-4 and col. 7, lines 34-44) using the specific common time reckonings present in the

plurality of variable delay networks (by adding the value of the cycle time register plus a specific

maximum time margin at the 1394 link 13 of PC 1 in the source packet header, see col. 7, lines

34-44), wherein the heterogeneous networks as a whole emulates a constant delay network (the

values of the cycle time registers at all the nodes are synchronous with the reference clock at the

root node, see col. 6, lines 28-37; note that the combination of the value of the cycle time register

and a specific maximum time margin is considered as a constant time delay); and

transmitting a multimedia packet over the heterogeneous networks (the transport packet

to which the correct source packet header has been added can be transmitted from the 1394 link

13 to the digital TV 2, see col. 8, lines 11-24).


Regarding claim 2, Ishibashi discloses a method in accordance with claim 1, further

comprising the following:

receiving the multimedia packet from a previous network in the heterogeneous networks

(digital TV, an external node, receives data from the 1394 interface section 13, see col. 6, lines

55-64);

as the multimedia packet transitions from the previous network (node that comprises PC

1) to a next network (external node that comprises digital TV) in the heterogeneous networks,

configuring the multimedia packet (time stamp adding section 124 in the digital broadcast

receiving section 12 to add the corresponding packet arrival time to each ATM cell as the time

stamp, see col. 6, lines 55-64) if necessary to conform with the requirements of the next network

if the multimedia packet does not already conform with the requirements of the next network

(CPU of PC1 extracts one program of transport streams and creates transport packets for only a

specific single program designated by the user and this is a process of converting TSPs (transport

packets) for programs into a TSP for a single program, see col. 7, lines 17-25); and

transmitting the reconfigured multimedia packet onto the next network (transmitting data

from the root node PC 1 to the external node digital TV, see col. 6, lines 40-67).


Regarding claim 3, Ishibashi discloses a method in accordance with Claim 2, further

comprising:

repeating the act of receiving the multimedia packet from a previous network, the act of

configuring the multimedia packet if necessary (second and subsequent transport packets are

received and the output control section adds the time difference between arrival time included in

each of these packets and the timestamp assigned to the first packet, see col. 7, lines 63-67 and

col. 8, lines 1-7), and the act of transmitting the reconfigured multimedia packet onto the next

network for each network transition as the multimedia packet traverses the heterogeneous

networks from the multimedia source to the multimedia sink (sending the resulting packet to the

external node via the 1394 Link 10, see co. 6, lines 18-27, col. 8, lines 51-61 and Fig. 1).


Regarding claim 4, Ishibashi discloses the method in accordance with Claim 2, wherein

the next network is a variable delay network, wherein the act of configuring the multimedia

packet if necessary comprises the following:

generate a time stamp that represents a time in accordance with a common time

reckoning of the variable delay network (the output control section 112 of the PC 1 reads the

cycle time register and adds a specific maximum time delay to the value of the cycle time

register to create a source packet header, see col. 7, lines 53-62); and

including the time stamp in the multimedia packet (adds the source packet header as a

time stamp to the first transport packet, see col. 7, lines 53-62).

Regarding claim 6, Ishibashi discloses the method in accordance with Claim 4, wherein

the act of including the time stamp in the multimedia packet comprises the following:

including the time stamp in the multimedia packet before control of the multimedia

packet transfers to the link layer associated with the next network (adds the source packet header

as a time stamp to the first transport packet before the packet is transmitted from the IEEE 1394

Link 13 to the digital TV 2, see col. 7, lines 53-62 and col. 8, lines 11-24; note that next network

is the node that comprises a digital TV 2 via the IEEE 1394 Link 10).

Regarding claim 7, Ishibashi discloses the method in accordance with Claim 6, wherein

the act of including the time stamp in the multimedia packet before control of the multimedia

packet transfers to the link layer comprises the following:

an application layer (timestamp adding section 124) including the time stamp in the

multimedia packet (timestamp adding section 124 for adding the corresponding packet arrival

time to each ATM cell as a time stamp before packet is forwarded to 1394 Link, see col. 6, lines

55-64 and Fig. 1).

Regarding claims 8 and 11, Ishibashi discloses a computer program product (software,

see col. 5, lines 44-61 and col. 7, lines 34-44) for use in a variable delay network (network that

comprises root node PC 1 and external node digital TV2, see Fig. 1) that includes a transmitter

(root node PC 1) and a receiver (external node digital TV2), a transmitter application associated

with the transmitter configured to transmit a stream of multimedia packets through a transmitter

link layer controller, over the variable delay network, through a receiver link layer controller to a

receiver application associated with the receiver, the transmitter link layer controller having an

undedicated variable delay interface with the transmitter application, the transmitter link layer

controller and the receiver link layer controller being substantially synchronized in accordance

with a common network time base, a method of the transmitter link layer controller (software of

the 1394 output control section, see element 112, Fig. 1) emulating a constant delay network

over the variable delay network (software of 1394 Link 13 for PC emulates the operation of time

adjusting circuit (pacer) specified by IEC 61883, see col. 2, lines 1-5 and col. 7, lines 34-44)

despite the undedicated variable delay interface (despite the 1394 Link 13 for PC is not provided

with a pacer have a hardware unit for adding a source packet header in hardware), causing the

transmitter link layer controller (the 1394 output control section, see element 112, Fig. 1) to

perform the method comprising the following:

receiving a first multimedia packet (first packet) from the transmitter application, the

first multimedia packet including a first transmitter application time stamp (time stamp (arrival

time) OAT is added to the first transport packet, see col. 7, lines 63-67), which represents the

relative time that the information in the first multimedia packet should be rendered by the

receiver application in accordance with a transmitter application time base (time stamp OAT

represents the original arrival time that should be rendered when creating the source packet

header timestamp as a timestamp to be transported to the digital TV 2, see col. 8, lines 1-24, and

Fig. 2C);

including in the first multimedia packet a first network time stamp (value of cycle time

register within the 1394 Link 13, see col. 7, lines 34-44 and Fig. 2C), which represents the

relative time that the information in the first multimedia packet should be rendered by the

receiver application in accordance with the common network time base (value of cycle time

register represents the original arrival time that should be rendered when creating the source

packet header timestamp as a timestamp to be transported to the digital TV 2, see col. 7, lines 34-

44, and Fig. 2C);

receiving data representing a frequency of the transmitter application time base (a

reference clock of the time stamp included in the source packet header has a frequency of 24.576

MHz, see col. 8, line 67 and col. 9, lines 1-8);

receiving a second multimedia packet (second packet) from the transmitter application,

the second multimedia packet including a second transmitter application time stamp (arrival time

of second packet, see col. 8, lines 1-8), which represents the relative time that the information in

the second multimedia packet should be rendered by the receiver application in accordance with

the transmitter application time base (arrival time of second packet represents the arrival time

that should be rendered when creating the source packet header timestamp as a timestamp to be

transported to the digital TV 2, see col. 7, lines 34-44, col. 8, lines 1-8, and Fig. 2C);

calculating a second network time stamp (calculating the New cycle Time NCT)

representing the relative time that the information in the second multimedia packet should be

rendered by the receiver application in accordance with the common network time base (New

Cycle Time represents the time difference between the arrival time of the second packet and the

stored Original Arrival Time OAT), the calculation based on the first transmitter application time

stamp, the second transmitter application time stamp, the frequency, and the first network time

stamp (NCT is based on the first packet arrival time OAT, second packet arrival time, the

frequency of the reference clock of the timestamp included in the source packet header, and

value of cycle time register, see col. 8, lines 1-24);

including the second network time stamp in the second multimedia packet (NCT is added

in the source packet header, see col. 8, lines 1-8);

dispatching the second multimedia packet to the receiver application (sends the resulting

packet to the 1394 Link 13 and eventually to digital TV2 via the 1394 Link 10, see col. 8, lines

1-24).


Regarding claim 10, Ishibashi discloses a method in accordance with Claim 8, wherein

including the second network time stamp in the second multimedia packet (adding value of the

cycle time register on arrival of the transport packet, see col. 7, lines 34-44) is performed in

accordance with the IEC 61883 protocol (according to the IEC-61883 standard, see col. 7, lines

34-44).


Regarding claim 12, Ishibashi discloses a computer program product in accordance with

Claim 11, wherein the computer-readable medium is one or more physical storage media (media

processor, see col. 5, lines 51-61).


Regarding claim 14, Ishibashi discloses a computer program product (software, see col.

5, lines 50-61) in accordance with Claim 11, wherein the computer-executable instructions

(software for processing media transport streams, see col. 5, lines 50-61) for including the

second network time stamp in the second multimedia packet (adding value of the cycle time

register on arrival of the transport packet, see col. 7, lines 34-44) is executed in accordance with

the IEC 61883-x protocol (according to the IEC-61883 standard, see col. 7, lines 34-44).


Regarding claims 15 and 17, Ishibashi discloses a computer program product (software,

see col. 5, lines 44-61 and col. 7, lines 34-44) for use in a variable delay network (network that

comprises root node PC 1 and external node digital TV2, see Fig. 1) that includes a transmitter

(root node PC 1) and a receiver (external node digital TV2), a transmitter application associated

with the transmitter configured to transmit a stream of multimedia packets through a transmitter

link layer controller, over the variable delay network, through a receiver link layer controller to a

receiver application associated with the receiver, a method of the transmitter emulating a

constant delay network over the variable delay network, the computer program product

comprising a computer readable medium having stored thereon computer-executable instructions

(the software for implementing the functions of the 1394 output control section, see col. 7, lines

34-44 and element 112, Fig. 1) for performing the method comprising the following:

storing a transmitter application time base in a register (storing reference clock in cycle

time register, see col. 6, lines 29-36);

periodically transmitting the transmitter application time base to one or more other

devices in the variable delay network (time adjustment information based on the reference clock

is periodically broadcast from the root node serving as a cycle master to all the other 1394 nodes,

see col. 6, lines 18-36);

including a transmitter application time stamp (arrival time OAT is added to the transport

packet) in a multimedia packet, the transmitter application time stamp representing the relative

time that the information in the multimedia packet should be rendered by the receiver application

(time stamp OAT represents the original arrival time that should be rendered when creating the

source packet header timestamp as a timestamp to be transported to the digital TV 2, see col. 8,

lines 1-24, and Fig. 2C); and

dispatching the multimedia packet to the receiver application (sends the resulting packet

to the 1394 Link 13 and eventually to digital TV2 via the 1394 Link 10, see col. 8, lines 1-24).


Regarding claim 18, Ishibashi discloses a computer program product in accordance with

Claim 17, wherein the computer-readable medium is one or more physical storage media (media

processor, see col. 5, lines 51-61).

*Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3.       Claims 5, 9, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishibashi

et al. (USP 6,778,537) in view of Joy et al. (USP 6,820,150).

Regarding claim 5, Ishibashi discloses all the aspects of the claimed invention set forth in

the rejection of claim 1 above. Ishibashi further discloses the output control section that executes

the time adjusting emulation function of claim 1 is IEEE 1394 compliant (see col. 7, lines 34-44

and Fig. 1). Ishibashi fails to explicitly show the method in accordance with Claim 4, wherein

the act of including the time stamp in the multimedia packet is performed by the link layer.

However, Joy discloses each 1394-compliant bus driver comprises an implementation of

the IEEE 1394 link layer protocol, which is well known in the art (see col. 5, lines 60-67).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to combine the time stamp creating method of Ishibashi using the IEEE

1394 link standard with the teaching of Joy in using the link layer protocol to implement the

IEEE 1394 complaint bus driver such that the act of including the time stamp in the multimedia

packet is performed by the link layer. The motivation to do so is to comply with the IEEE 1394

standard when transmitting and receiving IEEE 1394 formatted packets.

Regarding claim 9, Ishibashi discloses a method in accordance with Claim 8, where the

variable delay network is an IEEE 1394 compliant network (the root node that comprises PC 1 is

IEEE 1394 compliant, see col. 5, lines 61 and Fig. 1) and the undedicated variable

delay interface comprises a PCI interface (PCI bus, see col. 5, lines 61 and Fig. 1).

Ishibashi does not explicitly show the transmitter link layer controller (the 1394 output

control section, see element 112, Fig. 1) comprises an OHCI link layer controller. However, Joy

discloses each 1394-compliant bus driver comprises an Open Host Controller Interface (OHCI)

driver, which is well known in the art (see col. 5, lines 60-67).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to combine the time stamp creating method of Ishibashi using the IEEE

1394 link standard in the output control section of PC 1 with the teaching of Joy in using the

Open Host Controller Interface (OHCI) driver to implement the IEEE 1394 complaint bus driver

such that the IEEE 1394 output control section (transmitter link layer controller) comprises an

OHCI link layer controller. The motivation to do so is to comply with the IEEE 1394 standard

when transmitting and receiving IEEE 1394 formatted packets.


Regarding claim 13, Ishibashi discloses a computer program product (software, see col.

5, lines 50-61) in accordance with Claim 11, where the variable delay network is an IEEE 1394

compliant network (the root node that comprises PC 1 is IEEE 1394 compliant, see col. 5, lines

61 and Fig. 1) and the undedicated variable delay interface comprises a PCI interface (PCI bus,

see col. 5, lines 61 and Fig. 1).

Ishibashi does not explicitly show the transmitter link layer controller (the 1394 output

control section, see element 112, Fig. 1) comprises an OHCI link layer controller.

However, Joy discloses each 1394-compliant bus driver comprises an Open Host

Controller Interface (OHCI) driver, which is well known in the art (see col. 5, lines 60-67).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to combine the time stamp creating method of Ishibashi using the IEEE

1394 link standard in the output control section of PC 1 with the teaching of Joy in using the

Open Host Controller Interface (OHCI) driver to implement the IEEE 1394 complaint bus driver

such that the IEEE 1394 output control section (transmitter link layer controller) comprises an

OHCI link layer controller.  The motivation to do so is to comply with the IEEE 1394 standard

when transmitting and receiving IEEE 1394 formatted packets.


4.      Claims 16, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishibashi et

al. (USP 6,778,537) in view of Hulyalkar et al. (USP 6,347,084).

Regarding claim 16, Ishibashi discloses all the aspects of the claimed invention set forth

in the rejection of claim 15 above, except fails to explicitly show the method in accordance with

Claim 15, wherein the variable delay network is an IEEE 802.11 compliant network.

However, Hulyalkar discloses a method of timestamp synchronization in a wireless ATM

network that includes a control node and a plurality of other nodes that communicate with one

another where the timestamp interval is created in accordance with the IEEE 802.11 standard

(see col. 4, lines 61-67 and col. 3, lines 1-17).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to modify the time stamp creating method of Ishibashi using the IEEE 1394

link standard in the output control section of PC 1 with the teaching of using IEEE 802.11

standard when performing timestamp synchronization between the control node and all other

nodes. The motivation to do so is to permit the creation of a more flexible timestamp interval

instead of the fixed cycle time required in the IEEE 1394 standard.


Regarding claim 19, Ishibashi discloses all the aspects of the claimed invention set forth

in the rejection of claim 15 above, except fails to explicitly show a computer program product in

accordance with Claim 17, wherein the variable delay network is an IEEE 802.11 compliant

network.

However, Hulyalkar discloses a method of timestamp synchronization in a wireless ATM

network that includes a control node and a plurality of other nodes that communicate with one

another where the timestamp interval is created in accordance with the IEEE 802.11 standard

(see col. 4, lines 61-67 and col. 3, lines 1-17).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to modify the time stamp creating method of Ishibashi using the IEEE 1394

link standard in the output control section of PC 1 with the teaching of using IEEE 802.11

standard when performing timestamp synchronization between the control node and all other

nodes. The motivation to do so is to permit the creation of a more flexible timestamp interval

instead of the fixed cycle time required in the IEEE 1394 standard. wherein the variable delay

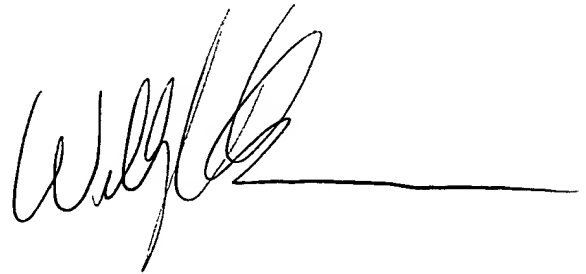network is an IEEE 802.11 compliant network.

## *Conclusion*

5.       The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure with respect to methods and systems for distributing multimedia data over

heterogeneous networks.

US Patent 6,661,810 to Skelly et al.

6.       Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Kevin Mew whose telephone number is 571-272-3141.  The

examiner can normally be reached on 9:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Wellington Chin can be reached on 571-272-3134.  The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system.  Status information for published applications

may be obtained from either Private PAIR or Public PAIR.  Status information for unpublished

applications is available through Private PAIR only.  For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KDM
Art Unit 2664